[0074] A direction of incidence of the ions may be substantially perpendicular to the surface of the substrate **301**. Therefore, a relatively large amount of ions may impinge at the top of the sidewall spacer structures **383**, **483**, whereas a relatively small amount of ions impinges at the bottom of the sidewall spacer structures **383**, **483**. Hence, the ion-implanted portions **384**, **484**, wherein the physical and/or chemical structure of the material of the sidewall spacer structures **318**, **418** is modified, are formed at the top of the sidewall spacer structures **318**, **418**, whereas the physical and/or chemical structure of the material of the sidewall spacer structures **383**, **483** may remain substantially unmodified or may be modified only to a lower extent at the bottom of the sidewall spacer structures **383**, **483**.

[0075] In addition to the ion-implanted portions **384**, **484** formed in the sidewall spacer structures **383**, **483**, further ion-implanted portions **385**, **386**, **387**, **388**, **389** may be formed in the liner layers **380**, **381** during the ion implantation process. The ion-implanted portions **385**, **386**, **387** are located over the stress-creating regions **314**, **315**, **414**, **415** and the trench isolation structure **302**. The ion-implanted portions **388**, **389** are located over the top surfaces of the gate electrodes **306**, **406**.

[0076] After the formation of the ion-implanted portions **385-389**, **384**, **484**, an etching process adapted to remove the ion-implanted portions **384**, **484** at a greater etch rate than other portions of the sidewall spacer structures **383**, **483**, such as, for example, portions of the sidewall spacers structures **383**, **483** at the bottom of the sidewall spacer structures **383**, **483**, and to remove the ion-implanted portions **385-389** in the liner layers **380**, **381** at a greater etch rate than the liner layers **380**, **381** when not irradiated with ions, may be performed.

[0077] In some embodiments, the etch process may comprise a wet etch process wherein the semiconductor structure **300** is exposed to an etchant which is adapted to remove the material of the liner layers **380**, **381**, and which is further adapted to affect the material of the sidewall spacers structures **318**, **383**. In some of these embodiments, the wet etchant may comprise hydrofluoric acid (HF). In other embodiments, a dry etch process may be used.

[0078] Since the physical and/or chemical structure of the material of the sidewall spacer structures **383**, **483** has been modified in the ion implantation process, the ion-irradiated portions **384**, **484** may be affected by the etchant to a greater extent than other portions of the sidewall spacer structures **383**, **483**. Therefore, a thickness of the sidewall spacer structures **383**, **484** may be reduced in the vicinity of the top surfaces of the gate electrodes **306**, **406**, whereas the thickness of the sidewall spacer structures **383**, **483** in the vicinity of the bottom of the sidewall structures **383**, **483** may be reduced to a less extent. Thus, the sidewall spacer structures **383**, **384** may obtain a tapered shape, as shown schematically in FIG. **2***d*.

[0079] Since the chemical structure of the liner layers **380**, **381** in the ion-irradiated portions **385-389** has been modified by the ion irradiation process, the liner layers **380**, **381** may be more efficiently removed from the semiconductor structure **300** than in embodiments wherein the ion irradiation process is omitted.

[0080] FIG. **2***d* shows a schematic cross-sectional view of the semiconductor structure **300** in a later stage of the manufacturing process. After the etch process, a layer **360** of a dielectric material may be formed over the semiconductor structure **300**. The layer **360** may, for example, comprise silicon nitride, and may be formed by means of deposition techniques well known to persons skilled in the art, such as chemical vapor deposition and/or plasma enhanced chemical vapor deposition. Parameters of the deposition process may be adapted such that the layer **360** is subject to a compressive stress. In other examples, the layer **360** may be subject to a tensile stress. Thus, the stress exerted by the stress-creating regions **314**, **315**, **414**, **415** to portions of the substrate **301** below the gate electrodes **306**, **406** may be modified. In embodiments wherein the stress-creating regions **314**, **315**, **414**, **415** are adapted to exert a compressive stress to portions of the substrate **301** below the gate electrodes **306**, **406**, a compressive intrinsic stress of the layer **360** may enhance the stress in the substrate portions, whereas a tensile intrinsic stress of the layer **360** may reduce the stress in the substrate portions. Conversely, in embodiments wherein the stress-creating regions **314**, **315**, **414**, **415** are adapted to exert a tensile stress to the substrate portions, the tensile stress may be reduced by providing the layer **360** with a compressive intrinsic stress, and may be enhanced by providing the layer **360** with a tensile intrinsic stress.

[0081] In further embodiments, the layer **360** may comprise a portion comprising one of a compressive intrinsic stress and a tensile intrinsic stress which is provided over the first transistor element **330** and a portion comprising the other of a compressive intrinsic stress and a tensile intrinsic stress provided over the second transistor element **430**. In such embodiments, the portions of the layer **360** may be formed sequentially. First, a compressively stressed layer of the dielectric material may be formed over the semiconductor structure **300**. Thereafter, a portion of the compressively stressed layer over one of the transistor elements **330**, **430** may be removed by means of known methods of photolithography and etching. Subsequently, a tensile stressed layer of the dielectric material may be deposited over the semiconductor structure **300**, and a portion of the tensile stressed layer over the other of the transistor elements **330**, **430** may be removed by means of photolithography and etching.

[0082] Since, as detailed above, the sidewall spacer structures **383**, **483** have obtained a tapered configuration in the etch process performed after the creation of the ion-implanted portions **384**, **484**, the space between the gate electrodes **306**, **406** may have a shape similar to that of a groove having sloped walls. Therefore, in the deposition process performed in the formation of the layer **360**, reactant gases may more efficiently enter the space between the gate electrodes **306**, **406** than in the method according to the state of the art described above with reference to FIGS. **1***a*-**1***d*. Thus, an undesirable formation of voids between the gate electrodes **306**, **406** may be advantageously avoided.

[0083] After the formation of the layer **306**, a further layer **365** of a dielectric material may be deposited over the semiconductor structure **300**, and contact vias **362**, **363**, **364** may be formed and filled with an electrically conductive material, such as tungsten, to provide electrical connections to the source region **321**, the gate electrode **306** and the drain region **322** of the first transistor element **330**. Similarly, contact vias **462**, **463**, **463** filled with electrically conductive material may be formed to provide electrical connections to the source region **421**, the gate electrode **406** and the drain region **422** of the second transistor element **430**. This may be done by means of known methods of photolithography, etching and